Dolphin Technology

DOLPHIN TECHNOLOGY PRODUCT OFFERING
I2C / I2S

I2C/I2S - PHY (HARD IP)

Dolphin Technology's hardened I2C/I2S PHY provides a complete physical interface between bus and core logic to make a device I2C/I2S compliant. It is fully compliant with the I2C and I2S specifications.

I2C/I2S - CONTROLLER (SOFT IP)

Dolphin's I2C/I2S controller is designed to quickly and easily integrate into any SoC, and is optimized to provide a complete solution when combined with Dolphin's I2C/I2S PHY IP.

It is designed for 0.85/1.05 core VDD and 1.8V VDDO with support for Standard-mode, Fast-mode, Fast-mode Plus, and High Speed bus protocols. This is a fail-safe IO (VDDO can be powered down) and can tolerate 1.8V at the pad.

	16nm FF+ FFC	28nm HP, HPx LP, ULP	40nm G, LP ULP	55nm GP, LP ULP, EF	65nm GP LP
Drive programmable	●	●	●	●	●
Multi-mode support	●	●	●	●	●
Built in JTAG support for Mentor/LogicVision models	●	●	●	●	●
NAND or XOR tree select	●	●	●	●	●
Int/Out Register option	●	●	●	●	●
Pull down and sustain option	●	●	●	●	●
1.8 oxide	●	●	●	●	●
Metastability removal	●	●	●	●	●
Noise filter	●	●	●	●	●
Bus Start/Stop, stuck low detection	●	●	●	●	●
Signals (SDA/SCL) generation with user-defined timing constraints	●	●	●	●	●
Clock (SCL) synchronization	●	●	●	●	●
Bus arbitration	●	●	●	●	●
Customized I2C IO:	●	●	●	●	●
• 1.8V / 2.5V oxide	●	●	●	●	●
• Multi-mode support	●	●	●	●	●
• Full power bus strapping based on metallization/top metal requirements (horizontal and vertical metallization option available from M6 and above)	●	●	●	●	●
• Available in Wirebond, Flip Chip and CUP configurations	●	●	●	●	●

Front End views are available under NDA. For more information, contact: sales@dolphin-ic.com

Dolphin Technology, Inc. 333 W Santa Clara Street, Suite 920 San Jose, CA 95113
www.dolphin-ic.com Tel: +1 (408) 392-0012 Fax: +1 (408) 392-0090